

CLAIMS

We Claim:

1           1.    A method of improving yield in a multiple way  
2    associative cache memory having a plurality of cache blocks  
3    each corresponding to one of the multiple ways, the method  
4    comprising:

5                determining whether a defect exists in any of the  
6    cache blocks; and

7                for each way, selectively disabling the way if the  
8    corresponding cache block is defective.

1           2.    The method of Claim 1, further comprising:

2                for each way, storing a way select value indicative  
3    of whether the corresponding cache block is defective.

1           3.    The method of Claim 1, further comprising:

2                operating the remaining, non-disabled cache blocks as  
3    a less-associative cache memory.

1           4.    The method of Claim 1, wherein during a cache read  
2    operation the disabling step comprises:

3                forcing a comparison between a requested tag address  
4    and tags corresponding to cache lines in the disabled  
5    cache block to a mismatch condition so that the disabled  
6    cache block is not selected for the cache read operation.

1           5.    The method of Claim 4, wherein the forcing step  
2    comprises:

3                comparing the requested tag address with tags  
4    corresponding to the disabled cache block;

5                generating, for each cache block, a match signal  
6    indicating the results of the comparing step; and

7 gating the match signals with corresponding way  
8 select values to selectively force the mismatch condition  
9 for comparison results corresponding to the disabled cache  
10 block.

1 6. The method of Claim 4, wherein during a cache write  
2 operation the disabling step comprises:  
3 configuring a cache replacement algorithm to never  
4 select the disabled cache block.

1 7. A method of improving yield in an N way associative  
2 cache memory having N cache blocks corresponding to the N ways,  
3 the method comprising:  
4 determining whether a defect exists in a cache block;  
5 disabling the cache block if there is a defect in the  
6 cache block; and  
7 operating the remaining cache blocks as an N-1 way  
8 associative cache memory.

1 8. The method of Claim 7, further comprising:  
2 storing a plurality of way select values, each  
3 indicating whether a corresponding cache block is to be  
4 disabled.

1 9. The method of Claim 8, wherein during a cache read  
2 operation the disabling step comprises:  
3 forcing a tag comparison corresponding to the  
4 disabled cache block to a mismatch condition.

1 10. The method of Claim 9, wherein the forcing step  
2 further comprises:  
3 comparing a requested tag address with tags

4 corresponding to the disabled cache block;  
 5 generating a match signal in response to the  
 6 comparing step; and  
 7 gating the match signal with a corresponding way  
 8 select value to selectively force the mismatch condition.

1 11. A multiple-way associative cache memory, comprising:  
 2 a plurality of cache blocks, each having a number of  
 3 cache lines to store data;  
 4 a plurality of tag arrays, each storing a number of  
 5 tags for associated data in a corresponding one of the  
 6 plurality of cache blocks; and  
 7 select means connected to both the cache blocks and  
 8 the tag arrays, the select means configured to selectively  
 9 disable one or more of the plurality of cache blocks.

1 12. The cache memory of Claim 11, wherein the select  
 2 means comprises:  
 3 a plurality of memory devices, each for storing a way  
 4 select value for a corresponding cache block;  
 5 a plurality of gating circuits, each having a first  
 6 input terminal coupled to receive a match signal from a  
 7 corresponding tag array, a second input terminal coupled  
 8 to receive a corresponding way select value, and having an  
 9 output terminal to provide a gated match signal for a  
 10 corresponding cache block.

1 13. The cache memory of Claim 12, further comprising:  
 2 an encoder circuit having a plurality of input  
 3 terminals coupled to receive the gated match signals for  
 4 corresponding cache blocks, and having an output terminal  
 5 to provide a select signal; and

6 a multiplexer having a plurality of input terminals  
7 coupled to receive data from corresponding cache blocks,  
8 an output terminal to provide output data, and a control  
9 terminal to receive the select signal.

1 14. The cache memory of Claim 13, wherein the select  
2 signal selects which cache block provides its data as the  
3 output data.

1 15. The cache memory of Claim 13, wherein the way select  
2 signals selectively disable corresponding cache blocks by  
3 forcing corresponding match signals to a mismatch condition.

1 16. The cache memory of Claim 12, wherein the memory  
2 devices comprise fuses.

1 17. The cache memory of Claim 12, wherein the gating  
2 circuits comprise AND gates.